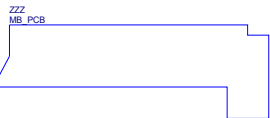


MODEL NAME : *VAZA0*
PCB NO : *LA-9262P (DAB0000I010)*
BOM P/N :

Dell/Compal Confidential

Schematic Document

Murcielgo MLK (Haswell ULT)

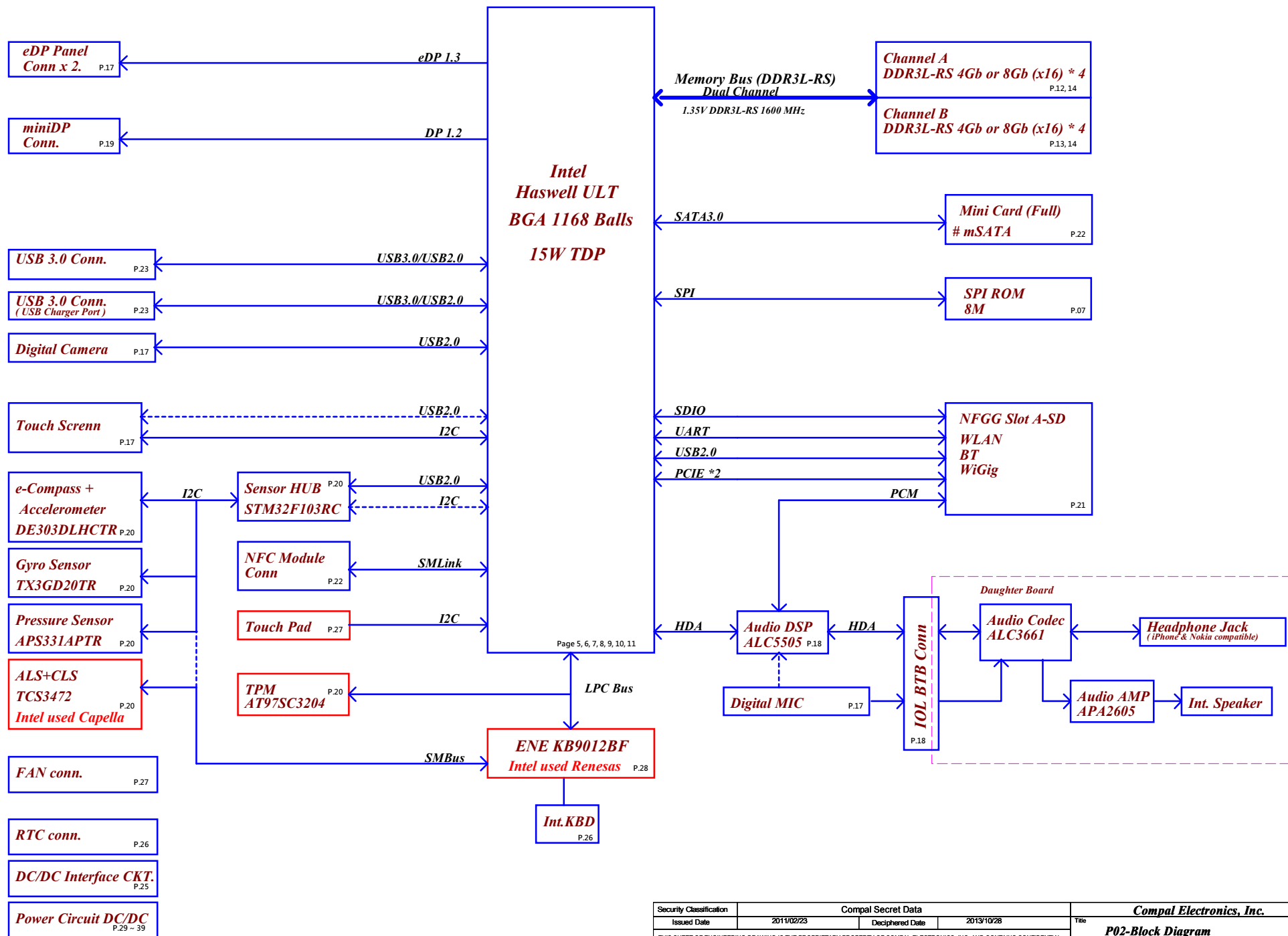


2013-04-19

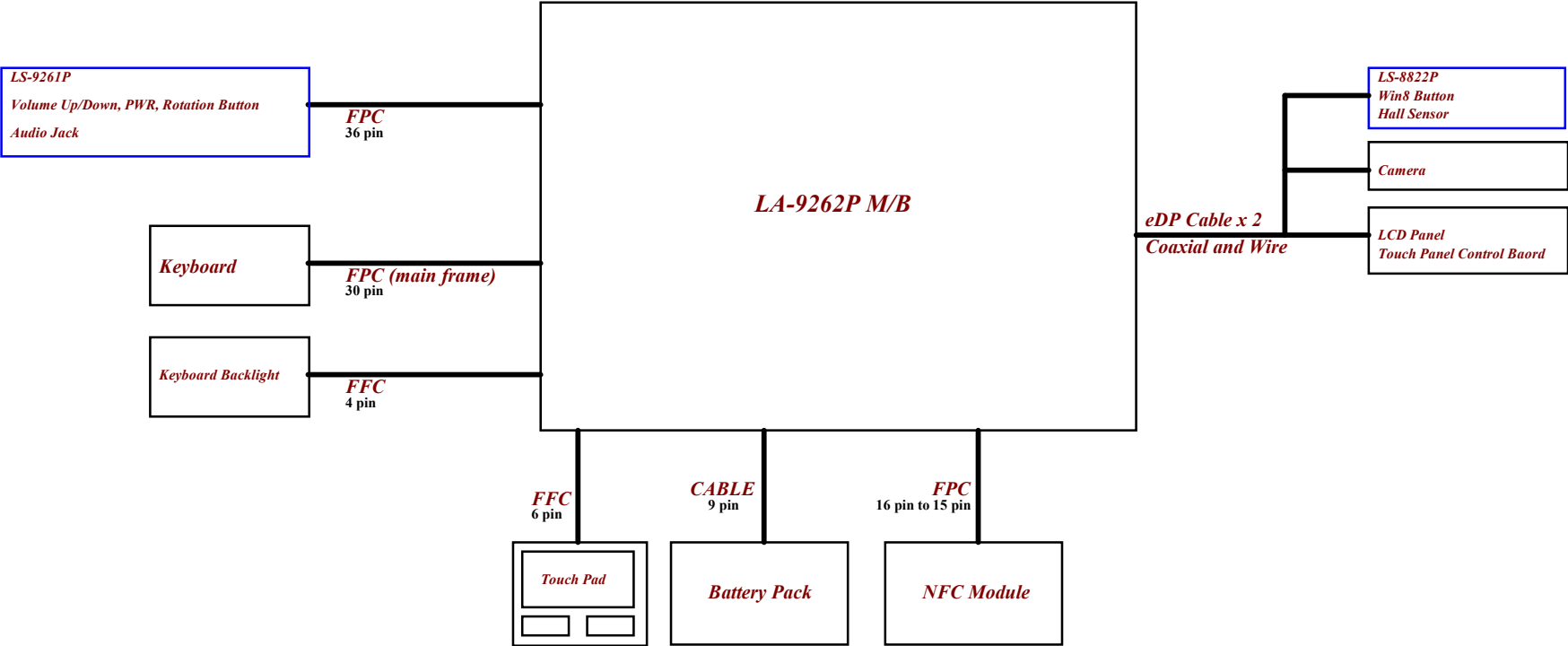
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Highlight the short pad for 0 ohm

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Project Code : VAZA0
File Name : LA-9262P



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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 1%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0				
1	12K +/- 1%				
2	15K +/- 1%				
3	20K +/- 1%				
4	27K +/- 1%				
5	33K +/- 1%				
6	43K +/- 1%				
7	56K +/- 1%				
8	75K +/- 1%				
9	100K +/- 1%				
10	130K +/- 1%				
11	160K +/- 1%				
12	200K +/- 1%				
13	240K +/- 1%				
14	270K +/- 1%				
15	330K +/- 1%				
16	430K +/- 1%				
17	560K +/- 1%				
18	750K +/- 1%				
19	NC				

BOARD ID Table

Board ID	PCB Revision
0	CS 0.1
1	CS 0.2
2	CS 0.3
3	CS 0.4
4	CS 0.5
5	CS 1.0
6	
7	
8	
9	
10	Non-CS 0.1
11	Non-CS 0.2
12	Non-CS 0.3
13	Non-CS 0.4
14	Non-CS 1.0
15	
16	
17	
18	
19	

PCH USB Port Mapping	USB PORT#	DESTINATION
	0	External USB3
	1	External USB3
	2	NGFF CARD WLAN
	3	Touch Panel
	4	Camera
	5	Sensors HUB
	6	
	7	

SMBUS Control Table

	SOURCE	NGFF	BATT	Charger	NFC	XDP	DDR3 SPD	ALS	Touch Pad
EC_SMB_CK1 EC_SMB_DA1	KB9012		V	V					
EC_SMB_CK2 EC_SMB_DA2	KB9012							V	
PCH_SMLCLK PCH_SMLDATA	PCH	V			V				
PCH_SMLCLK PCH_SMLDATA	PCH								
MEM_SMBCLK MEM_SMBDATA	PCH					V	V		V

Link

PCH DDI Port Mapping	DDI PORT#	DESTINATION
	B	mini-DP
	C	

CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0		CLKOUT_LPC_0	EC LPC
	CLKOUT_PCIE1		CLKOUT_LPC_1	TPM
	CLKOUT_PCIE2			
	CLKOUT_PCIE3	NGFF CARD WLAN		
	CLKOUT_PCIE4			
	CLKOUT_PCIE5			

SATA	DESTINATION
SATA0	m-SATA
SATA1	
SATA2	
SATA3	

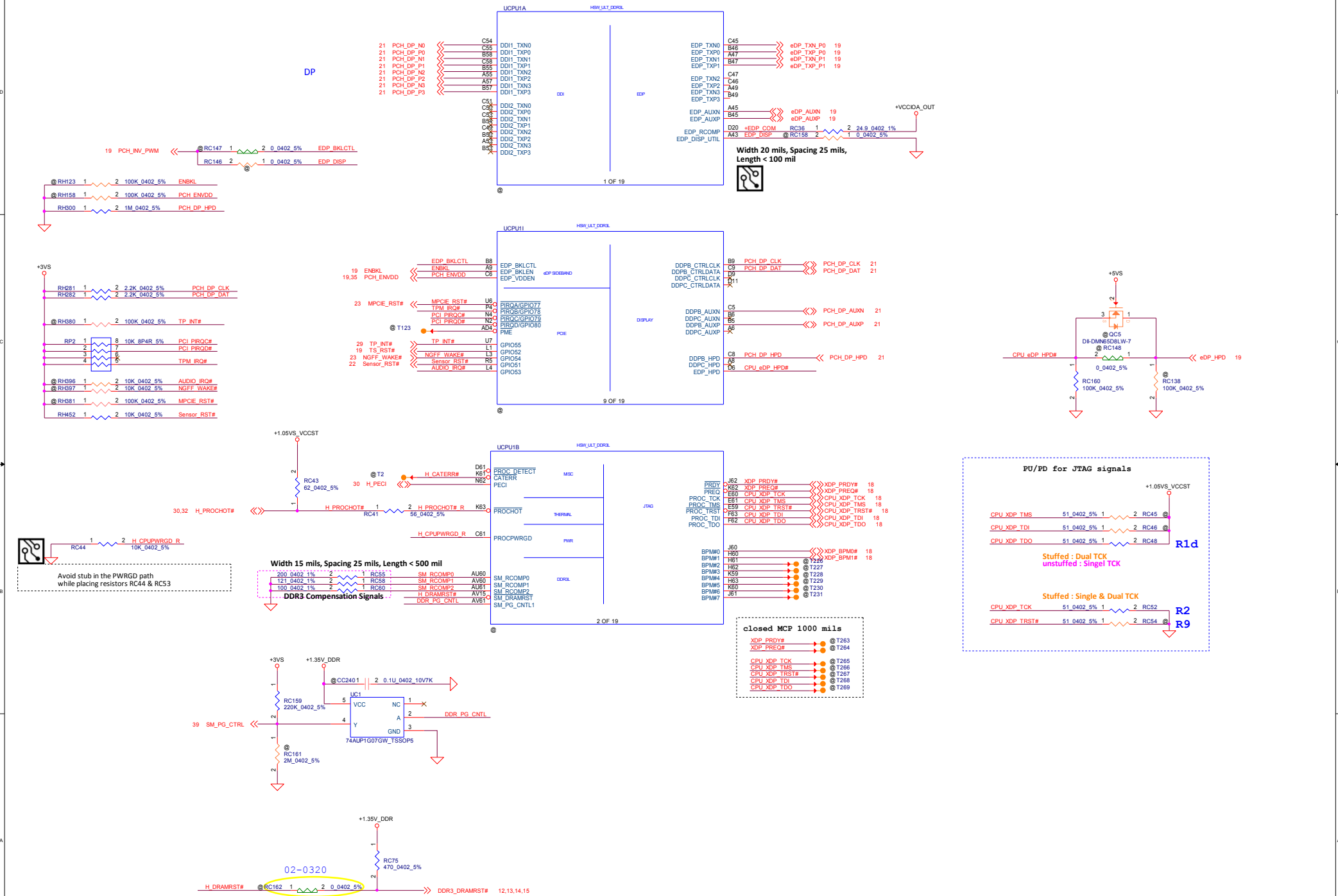
PCI EXPRESS	DESTINATION
Lane 1	
Lane 2	
Lane 3	NGFF CARD WLAN
Lane 4	NGFF CARD WLAN
Lane 5	
Lane 6	

Symbol Note :

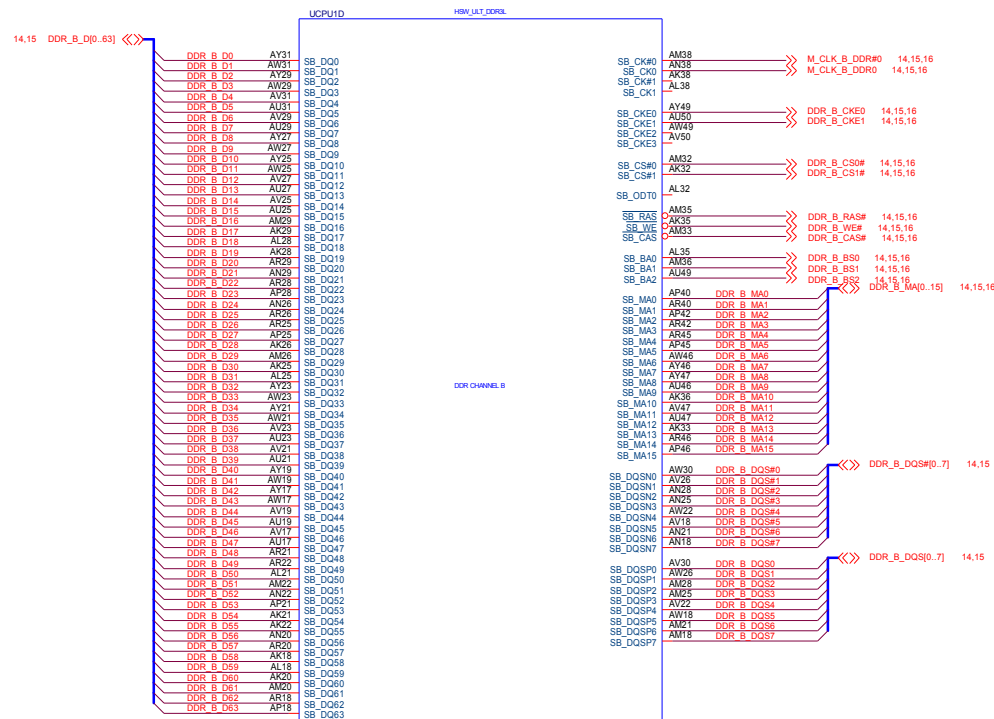
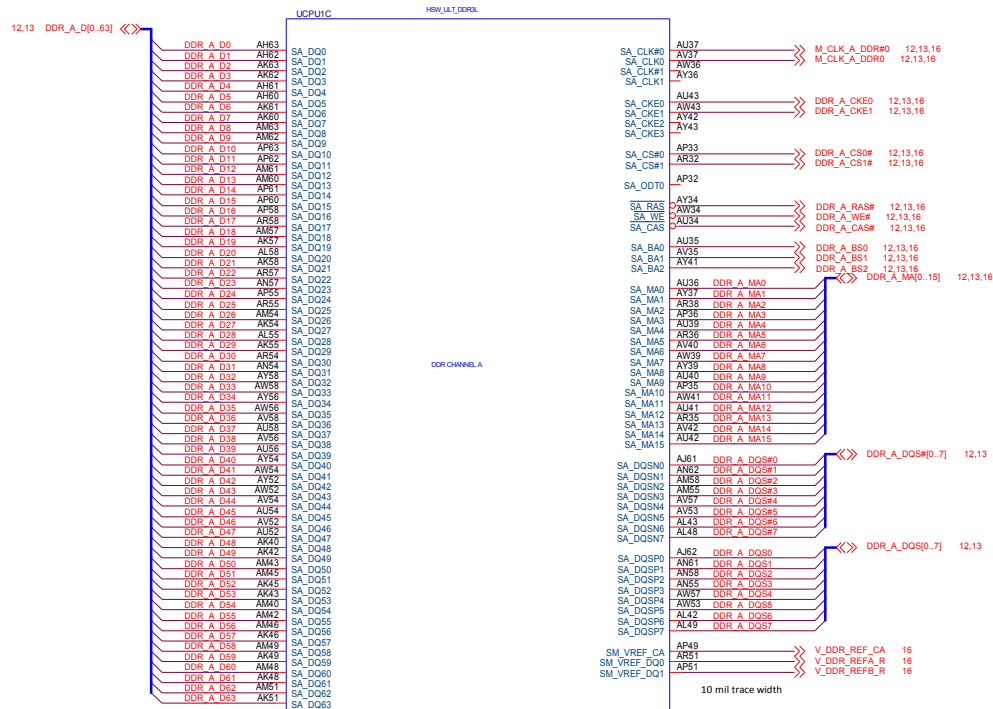
 : means Digital Ground

 : means Analog Ground

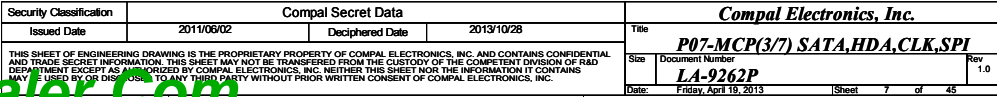
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Date				Friday April 19, 2013	Sheet	4 of 45

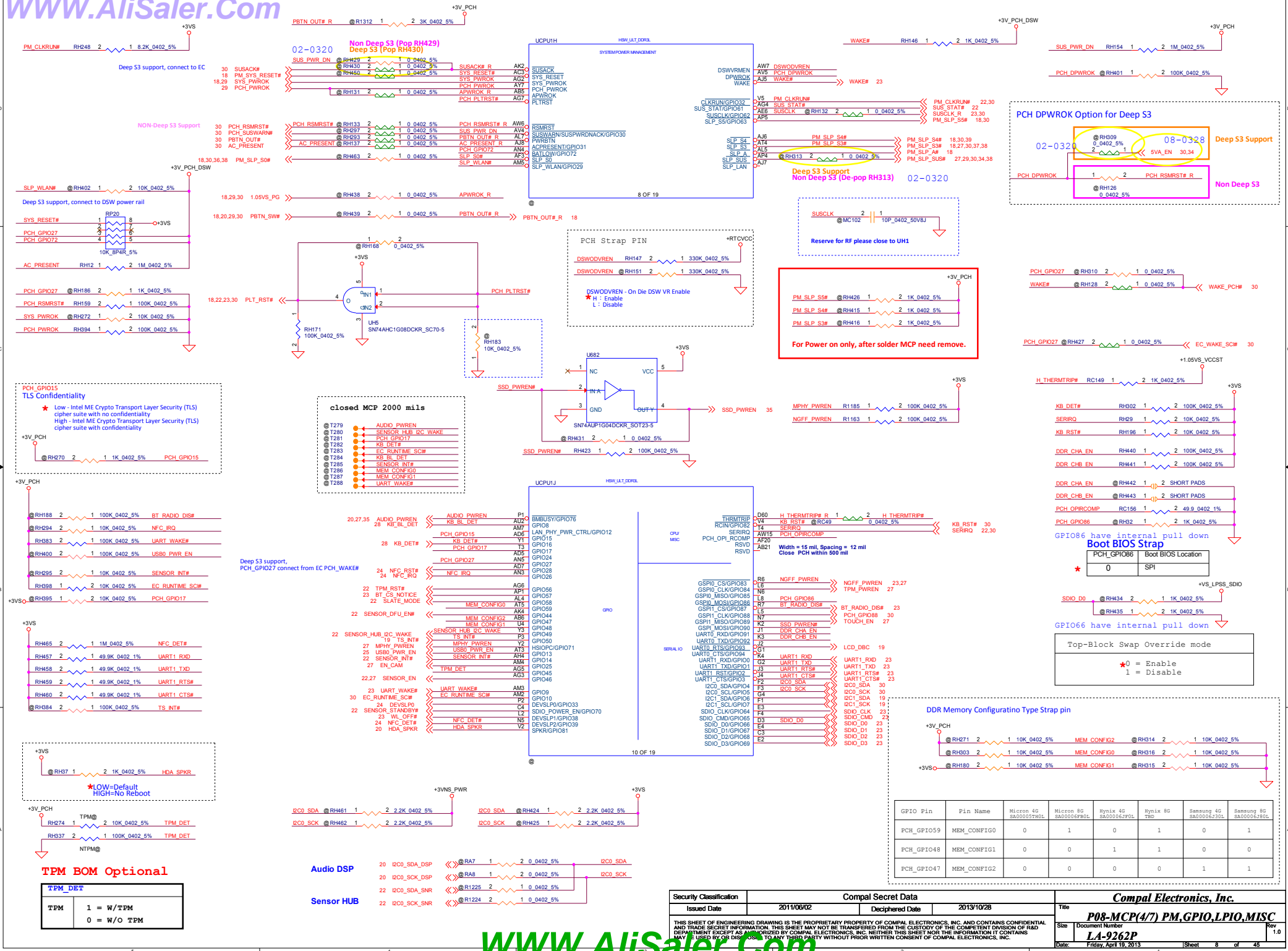


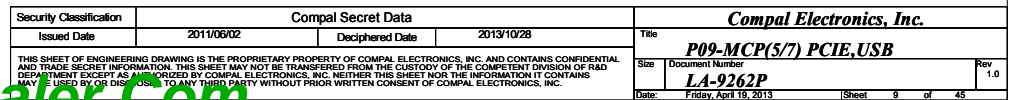
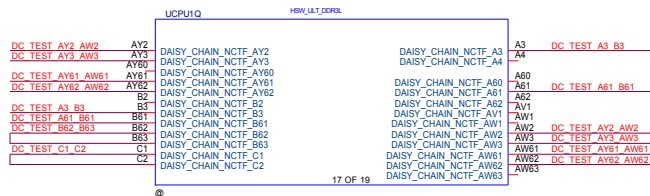
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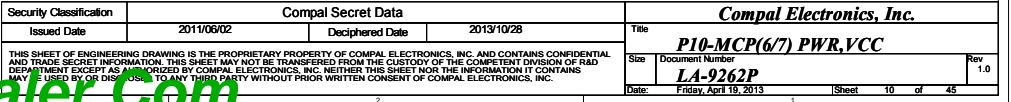


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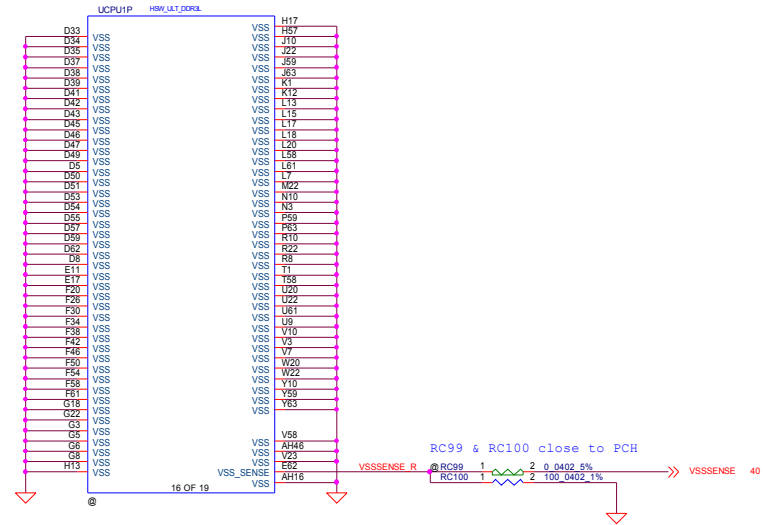
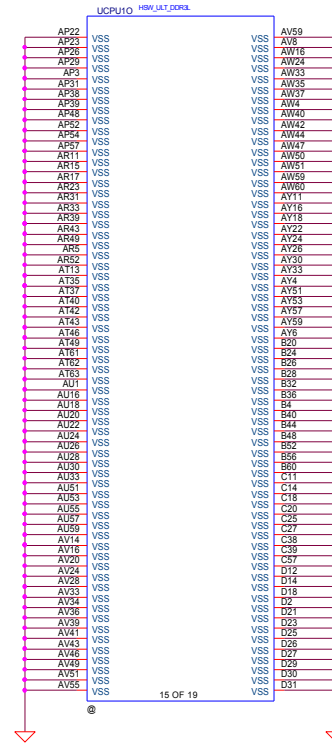
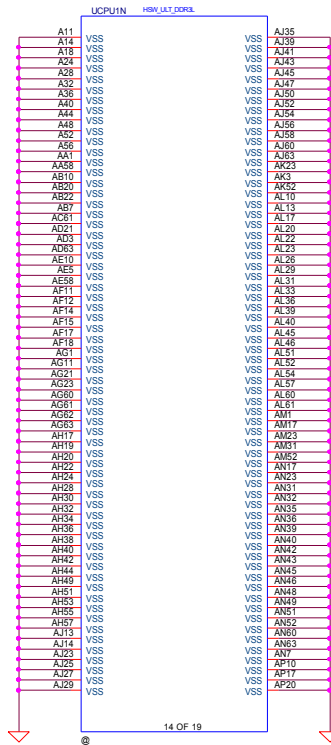
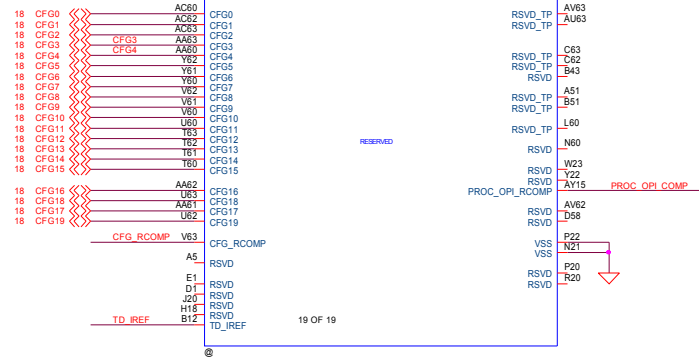
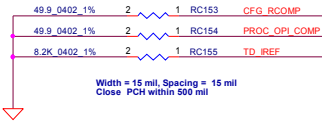
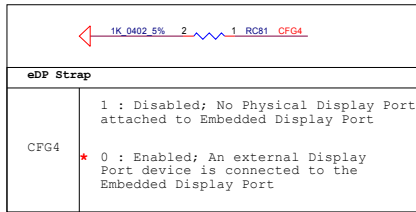






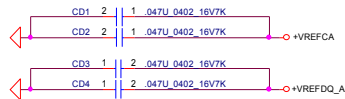
closed MCP 1000 mils

@ T293



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Size	Document Number	Rev	1.0	Sheet
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follow INTEL PDG

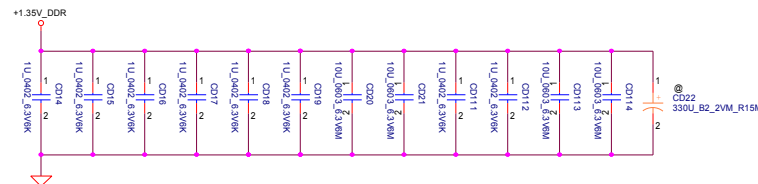
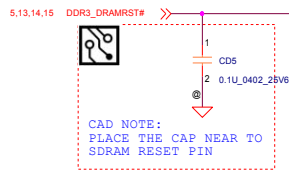
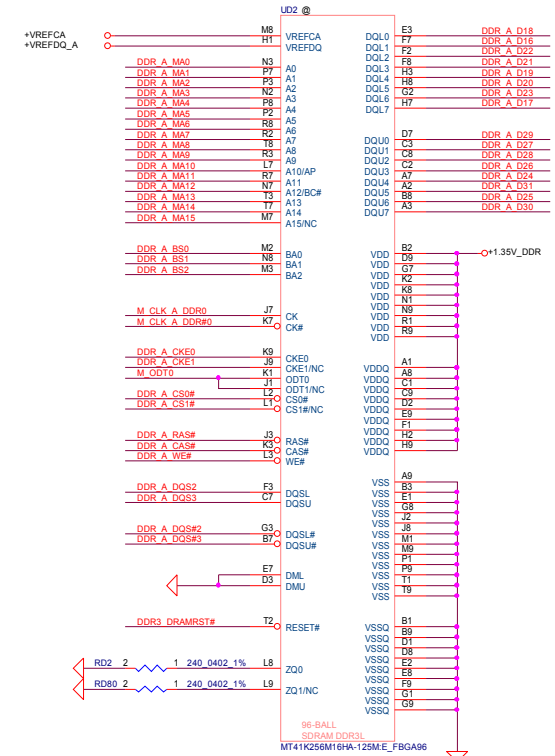
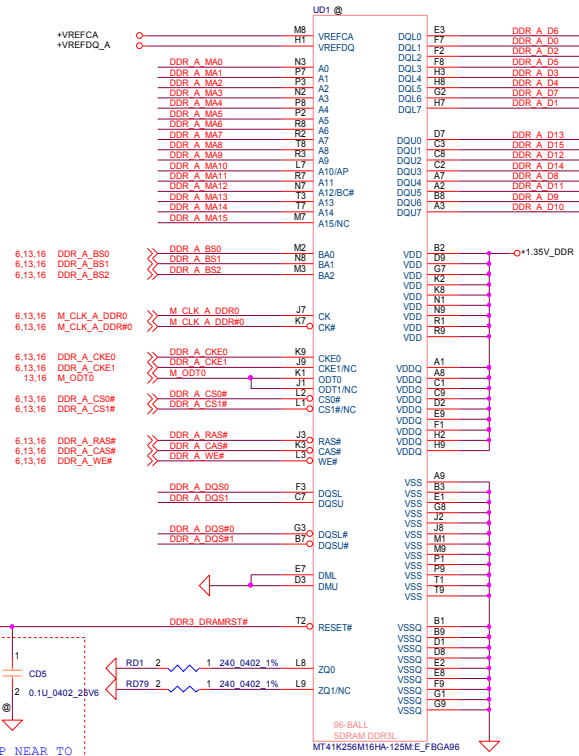


PLACE THESE CAPS
NEAR TO RESPECTIVE DIMM PINS

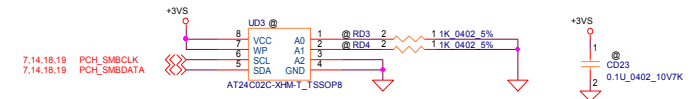


6.13 DDR_A_DQS#(0..7) <<>
6.13 DDR_A_DQS(0..7) <<>
6.13 DDR_A_D(0..63) <<>
6.13.16 DDR_A_MA(0..15) <<>

All VREF traces should
have 10 mil trace width



Memory Channel A SPD EEPROM



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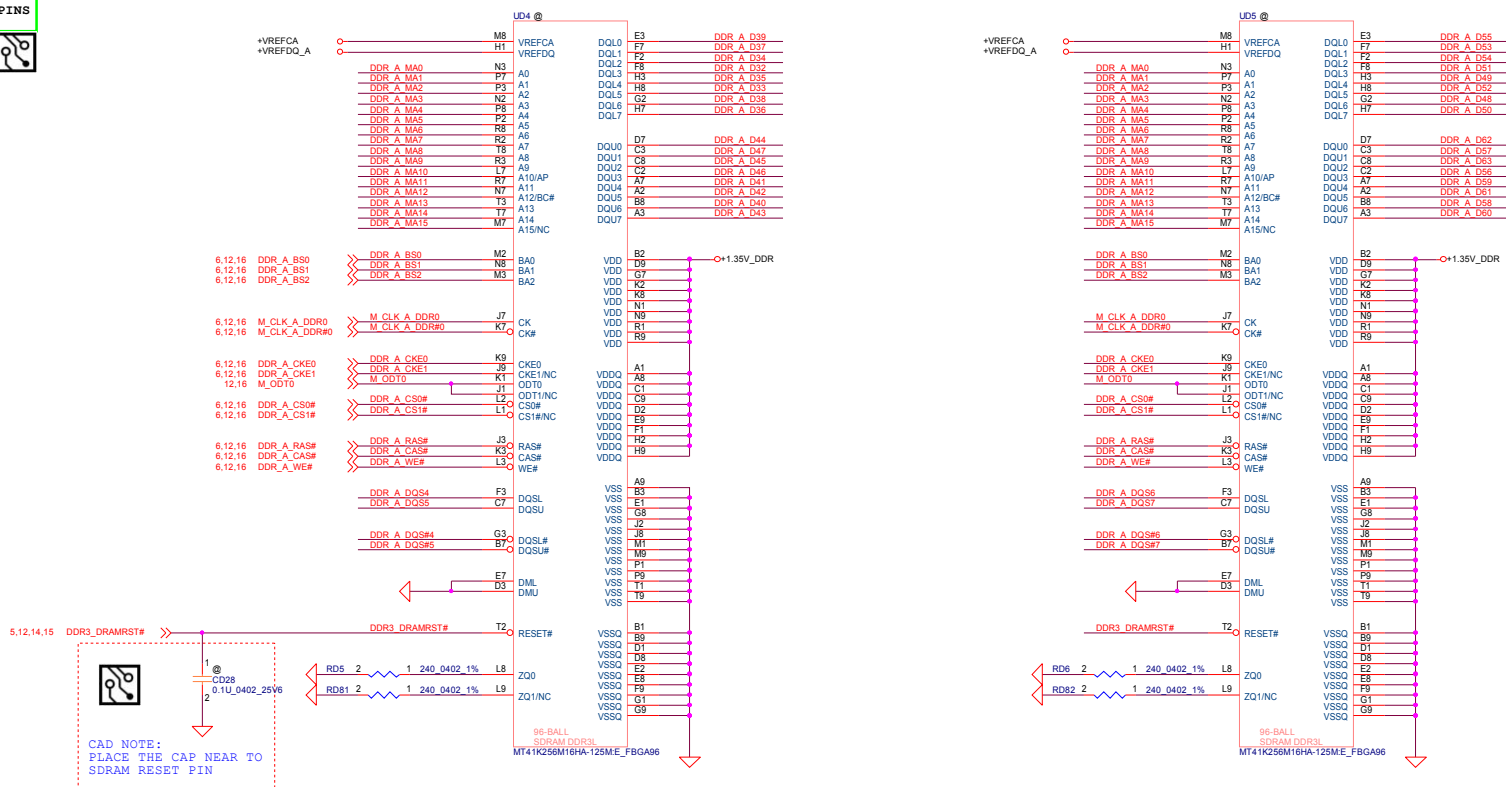


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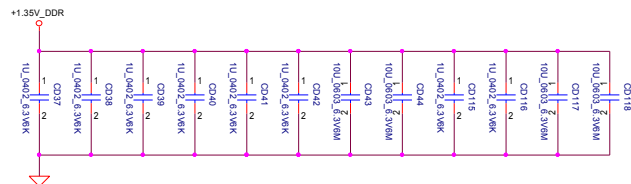


6.12 DDR_A_DQS#(0..7) <<>>
6.12 DDR_A_DQS(0..7) <<>>
6.12 DDR_A_D(0..63) <<>>
6.12,16 DDR_A_MA(0..15) <<>>

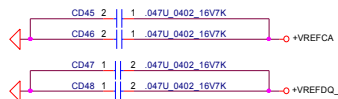
All VREF traces should
have 10 mil trace width



CAD NOTE:
PLACE THE CAP NEAR TO
SDRAM RESET PIN



follow INTEL PDG

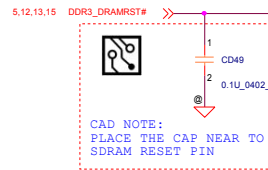
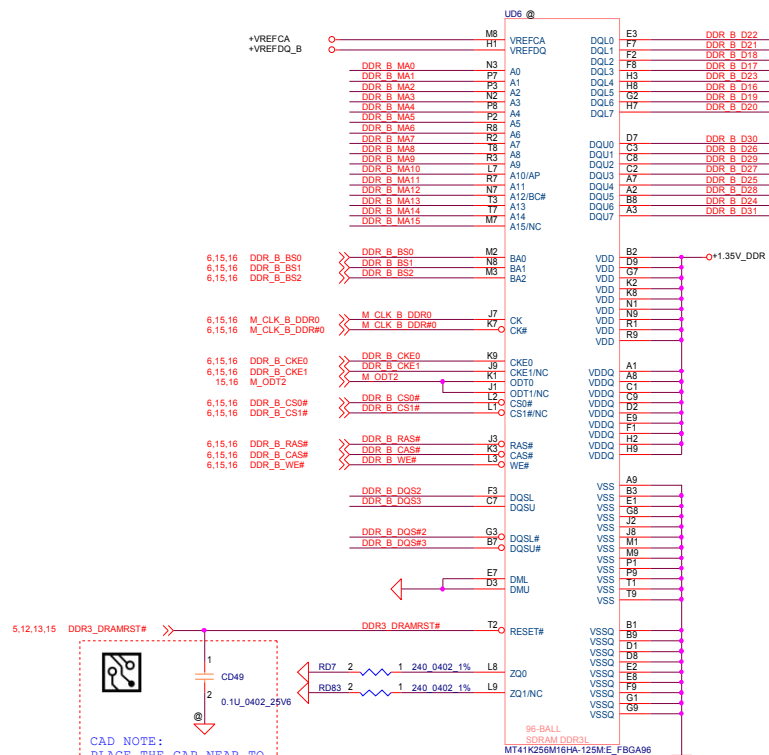


PLACE THESE CAPS
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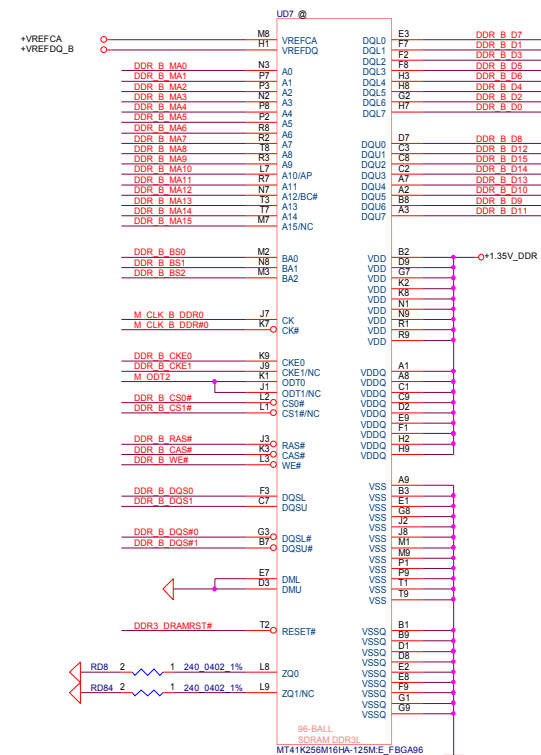


- 6.15 DDR_B_DQS#(0..7) <<>>
- 6.15 DDR_B_DQS(0..7) <<>>
- 6.15 DDR_B_Q(0..63) <<>>
- 6.15,16 DDR_B_MA(0..15) <<>>

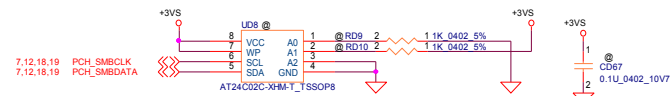
All VREF traces should
have 10 mil trace width



CAD NOTE:
PLACE THE CAP NEAR TO
SDRAM RESET PIN



Memory Channel B SPD EEPROM

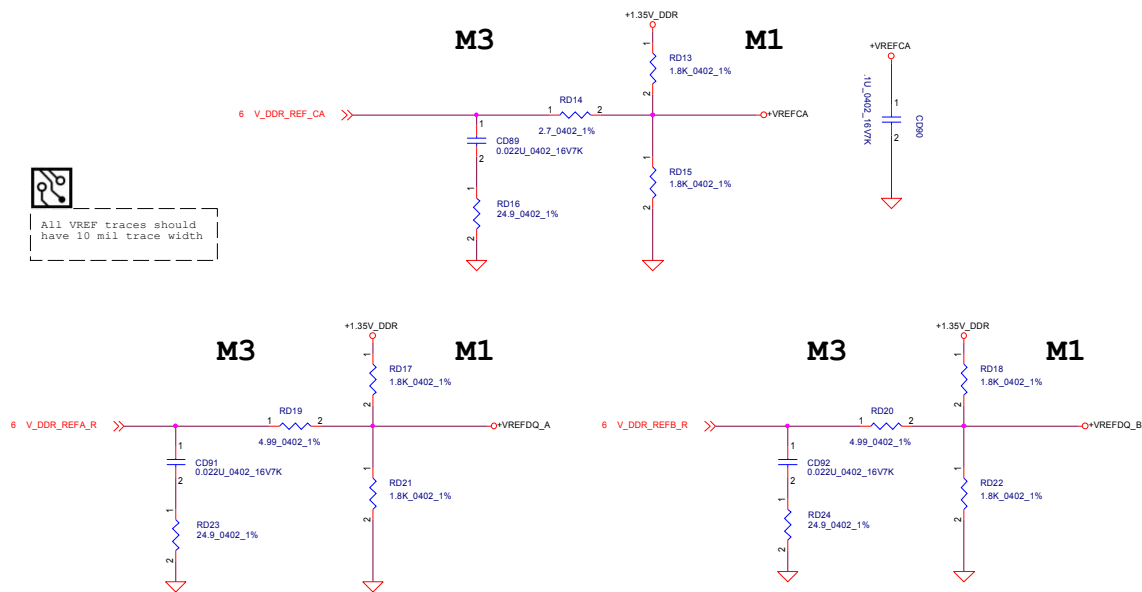


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P14-DDRIII Channel B Lower				
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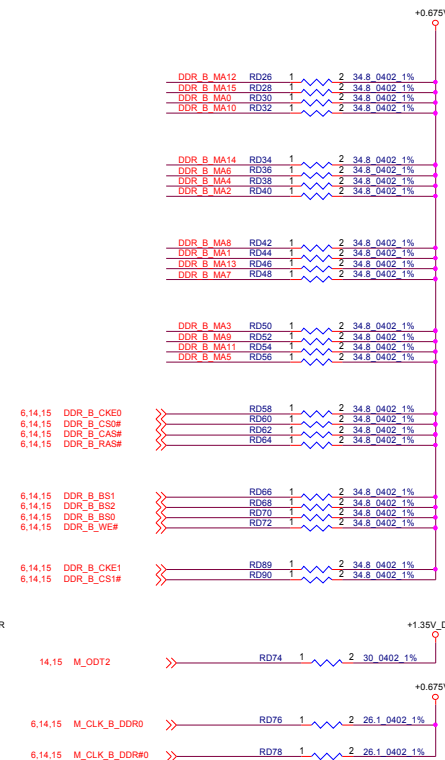
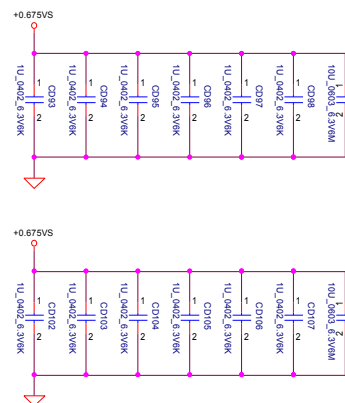
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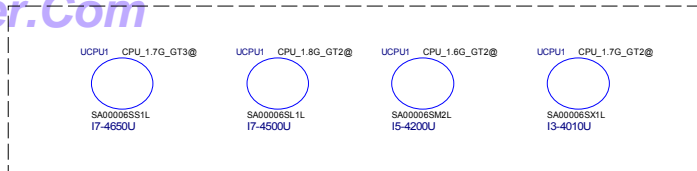
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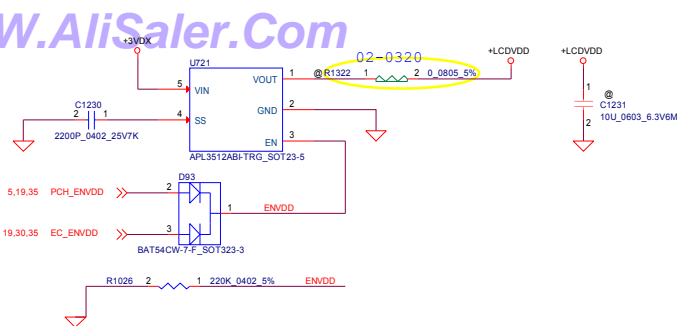
6.12.13 DDR_A_MA[0..15] <<>
6.14.15 DDR_B_MA[0..15] <<>



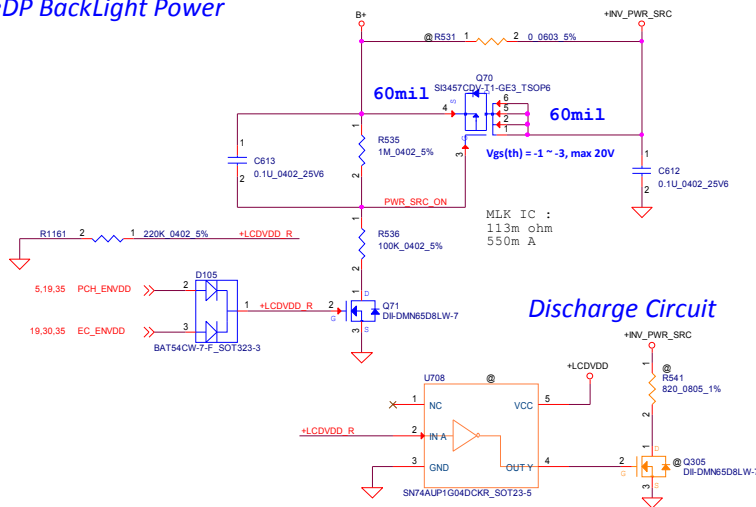
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12.13 M_ODT0		14.15 M_ODT2		1.0	
6.12.13 M_CLK_A_DDR0		6.14.15 M_CLK_B_DDR0		Date: Friday, April 19, 2013	
6.12.13 M_CLK_A_DDR#0		6.14.15 M_CLK_B_DDR#0		Sheet 16 of 45	



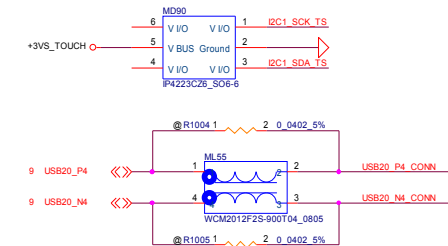
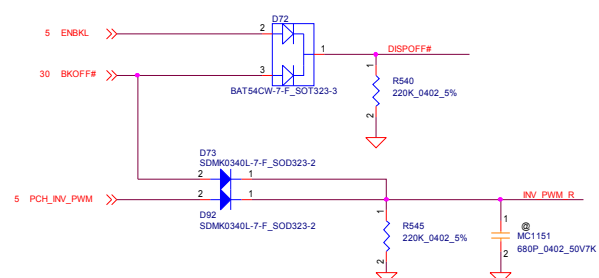




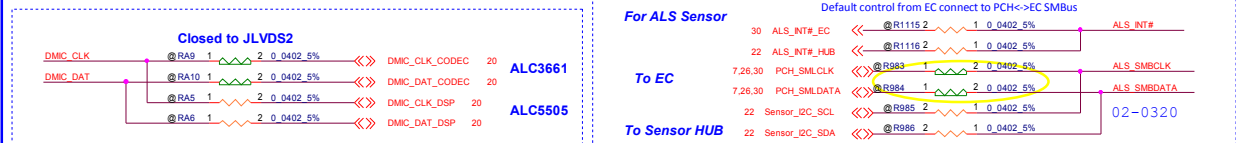
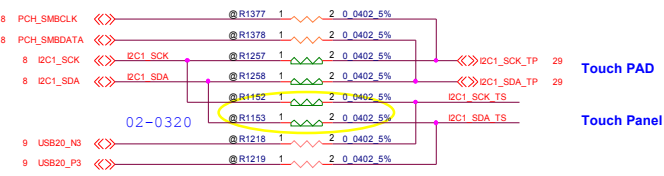
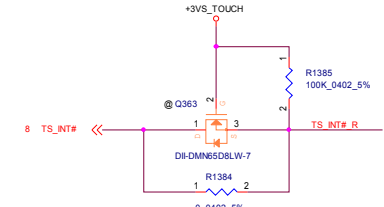
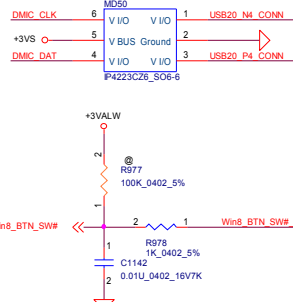
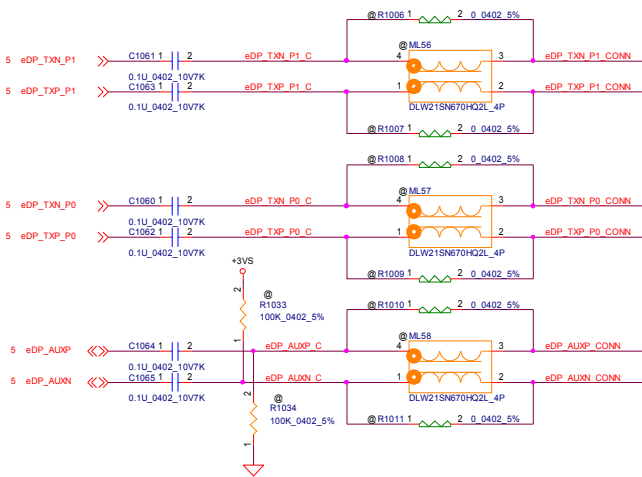
eDP BackLight Power



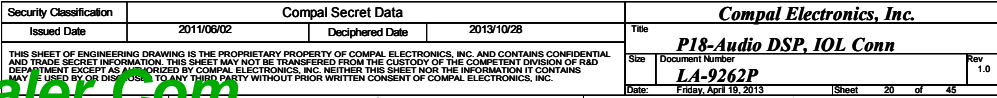
BackLight PWM Control

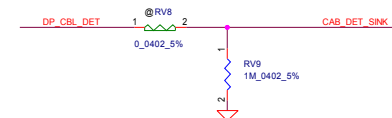


eDP Conn

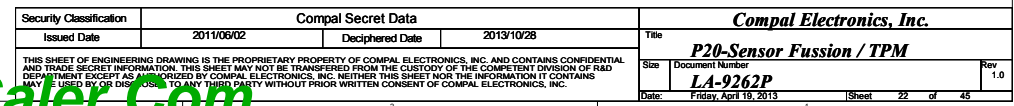


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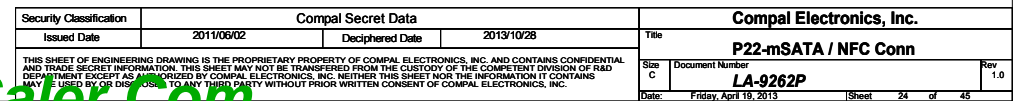
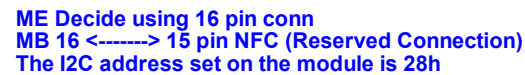


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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P19-Mini DP CONN
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				Document Number LA-9262P	
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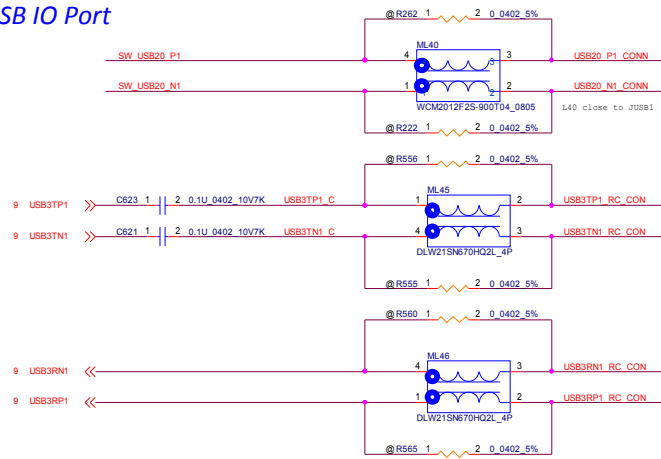




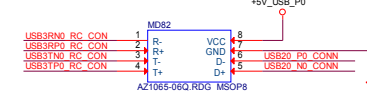
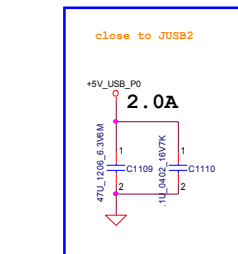
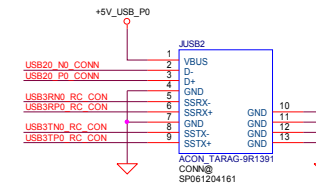
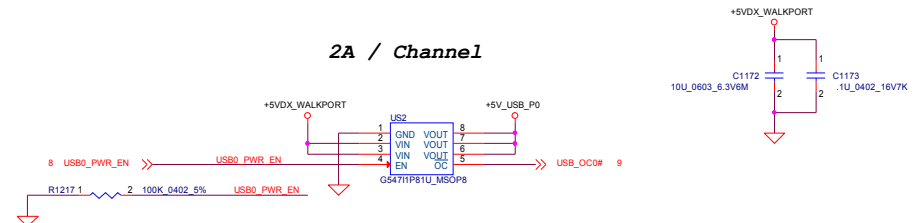
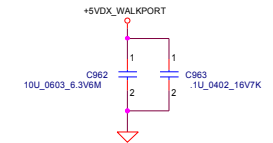
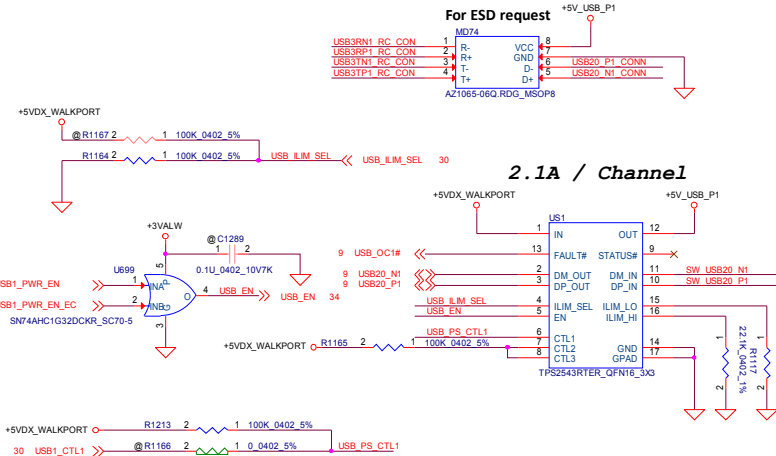
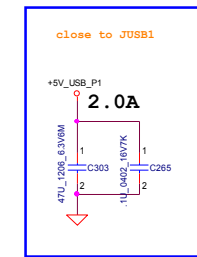
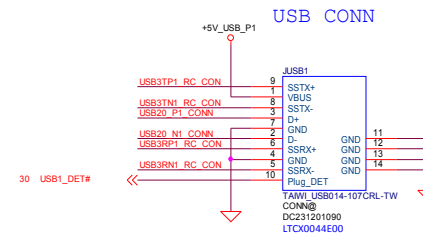
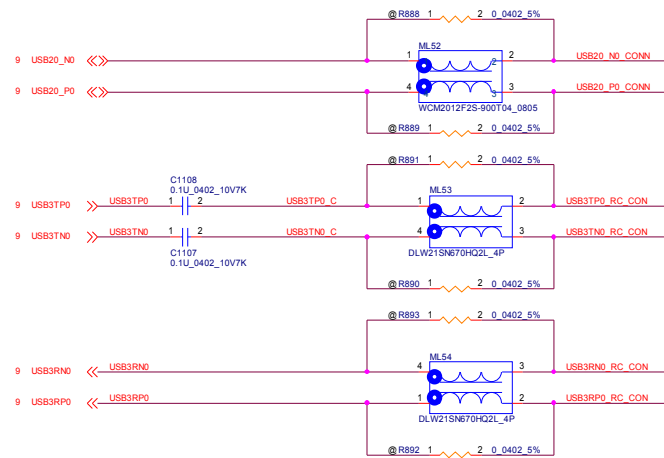
Security Classification		Compal Secret Data		Compal Electronics, Inc. P21-WLAN / WiGig / BT	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	
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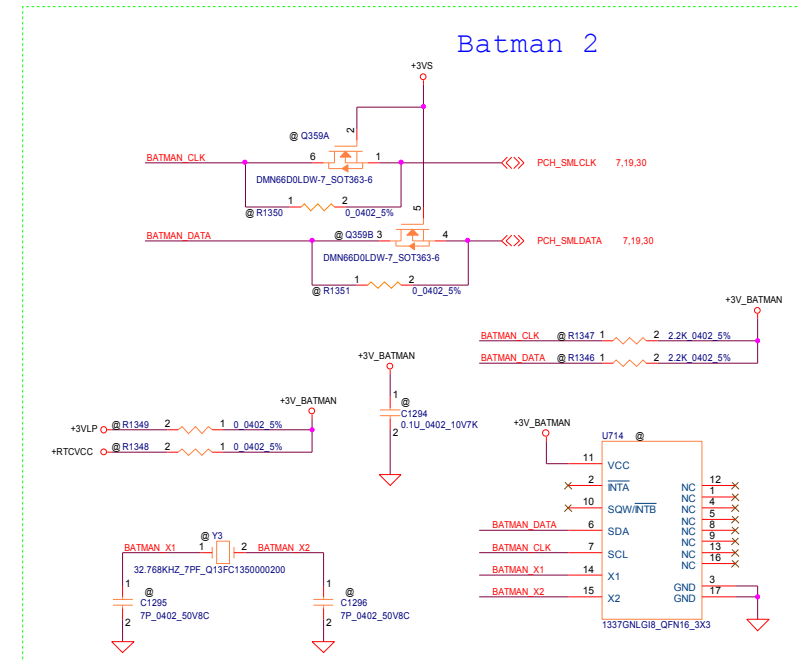
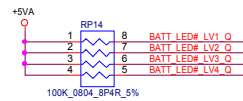
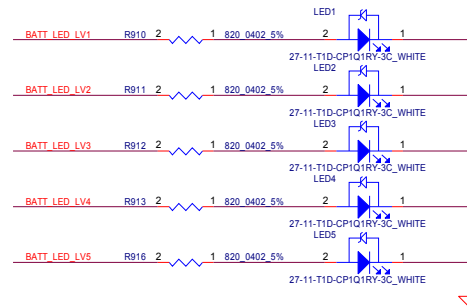
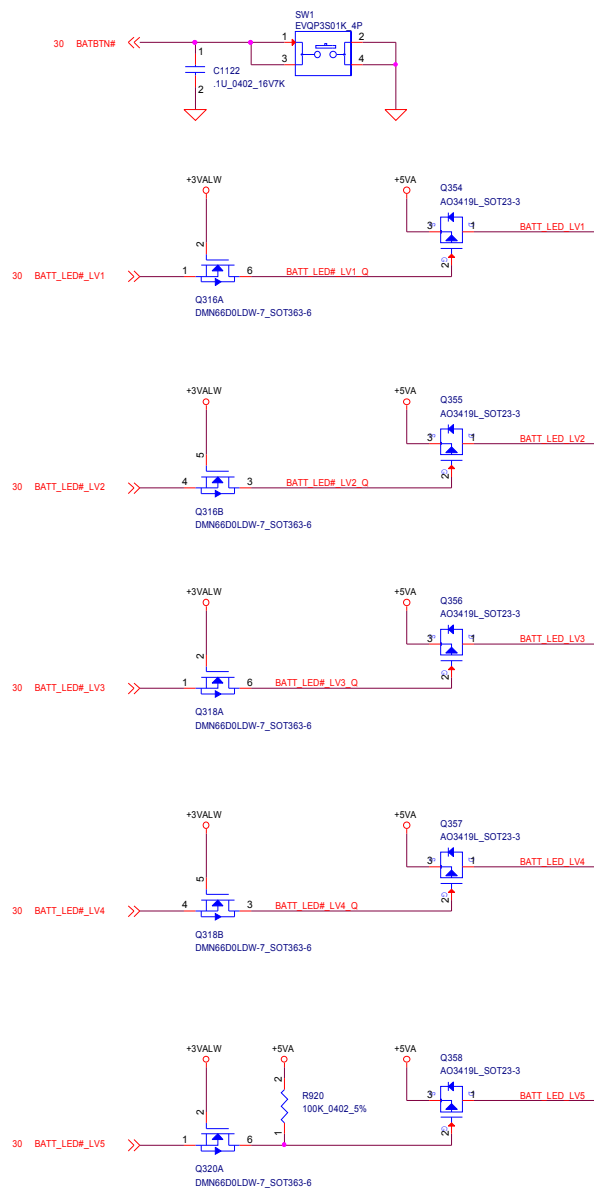
USB IO Port



CTL1	CTL2	CTL3	ILIM_SEL	MODE
0	1	1	0	DCP_Auto
0	1	1	1	DCP_Auto
1	1	1	0	SDF
1	1	1	1	CDP



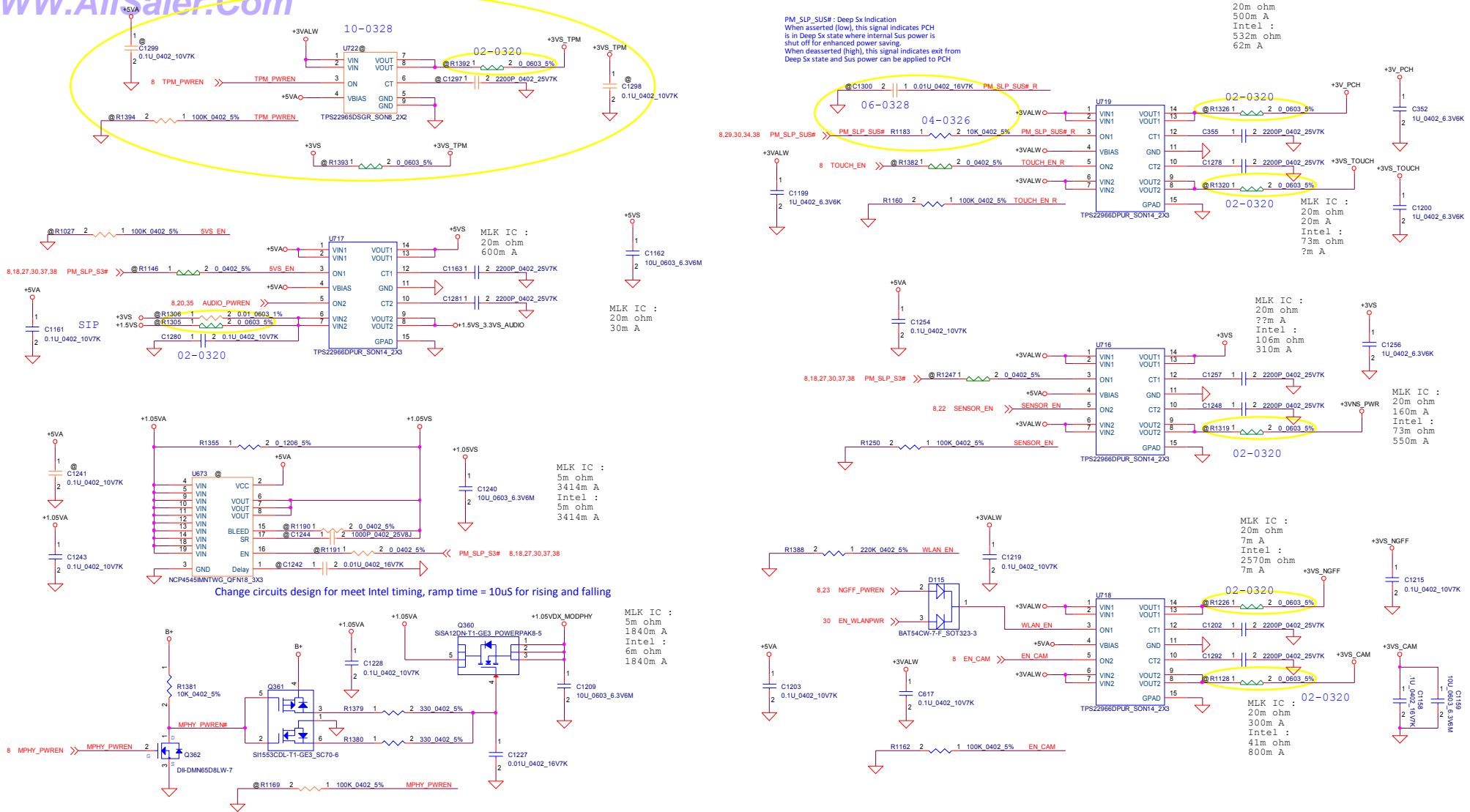
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	P23-USB 3.0 IO CONN
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title
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Size	Document Number	Rev		1.0
Date:	Friday, April 19, 2013	Sheet	26	of 45

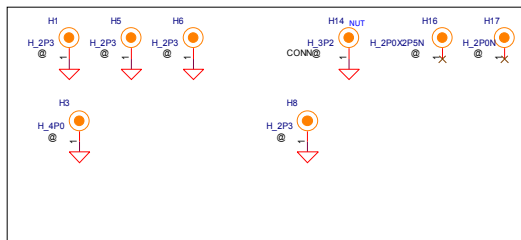
PM_SLP_SUS# : Deep Sx Indication
When asserted (low), this signal indicates PCH is in Deep Sx state where internal SLP power is shut off for enhanced power saving.
When deasserted (high), this signal indicates exit from Deep Sx state and SLP power can be applied to PCH

MLK IC :
20m ohm
500m A
Intel :
532m ohm
62m A

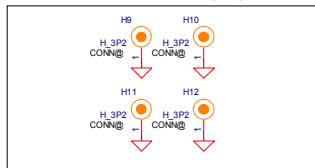




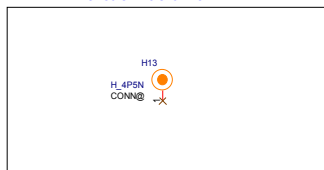
PCB Screw Hole



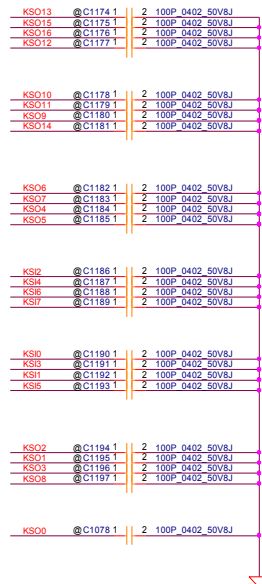
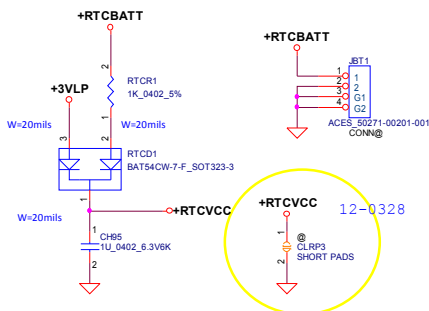
PCB Screw Hole for CPU (NUT)



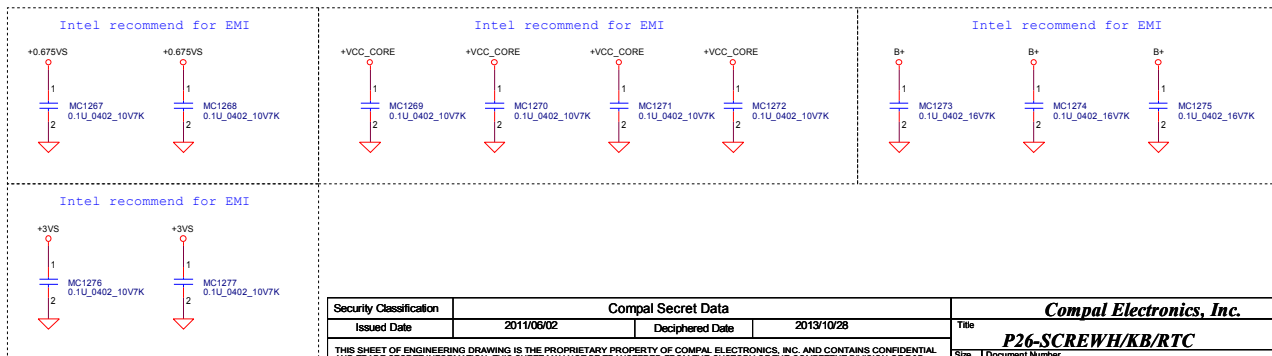
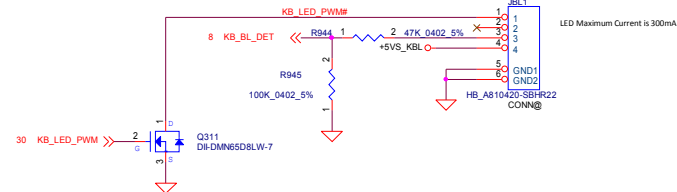
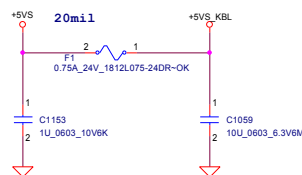
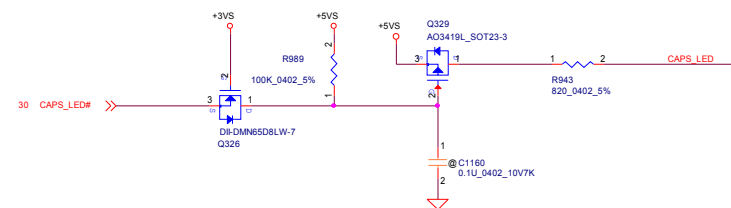
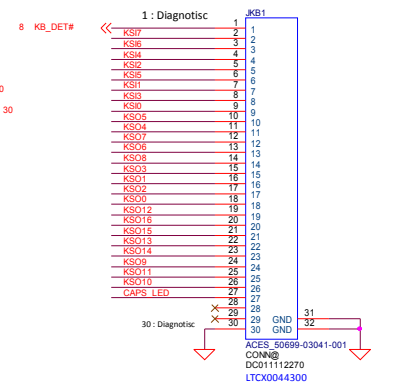
PCB Screw Hole for mSATA



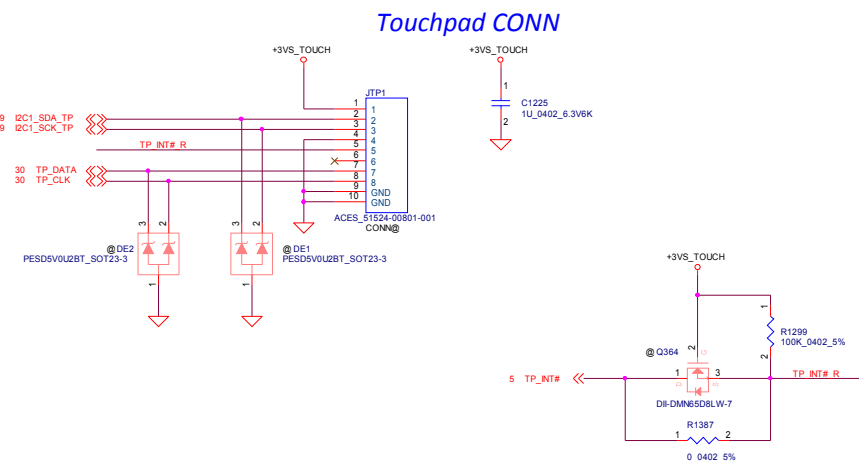
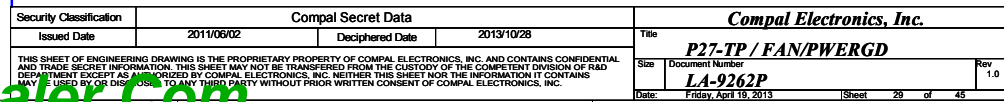
RTC Battery

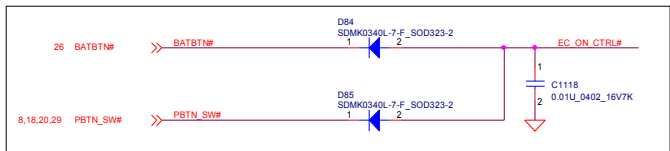
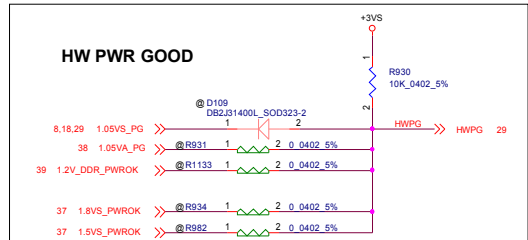
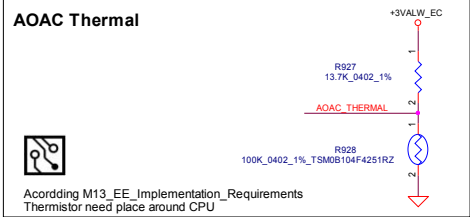


INT_KBD Conn.

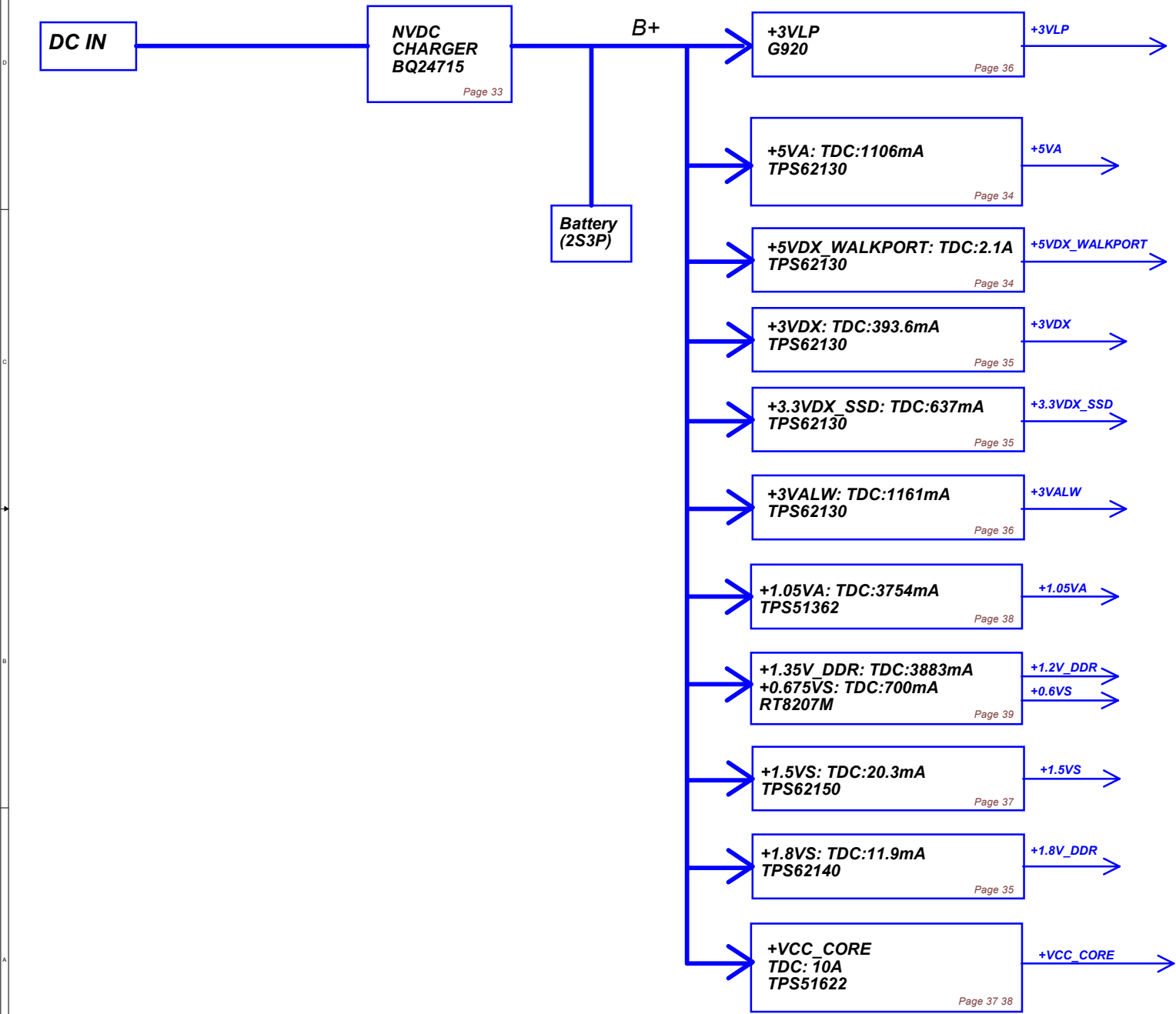


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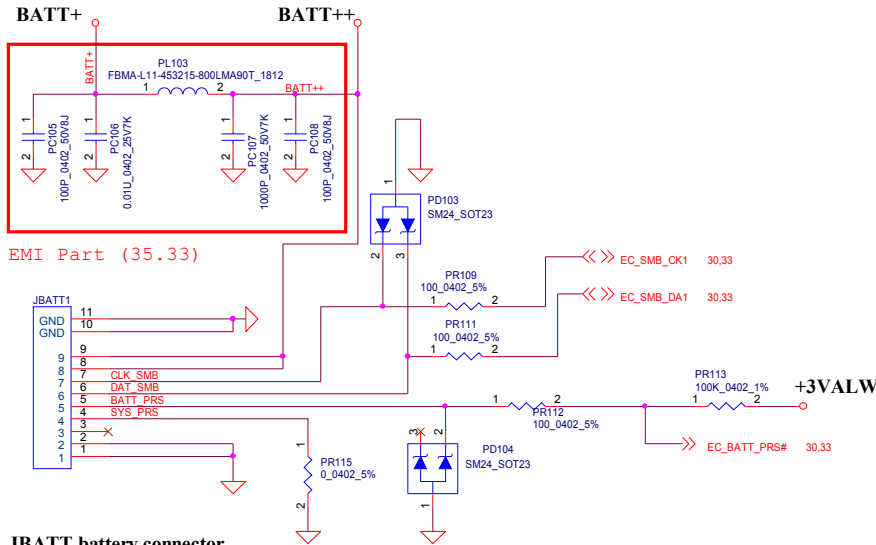
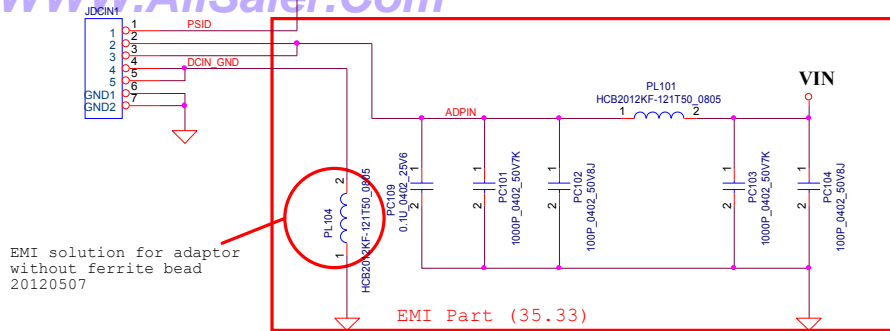




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				Date:	Friday, April 19, 2013	Sheet 30 of 45



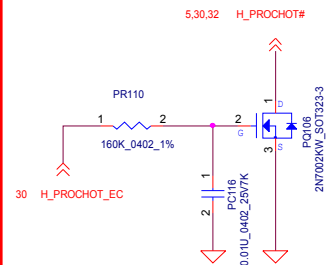
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Issued Date	2011/09/02	Deciphered Date	2013/10/28	Title	
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JBATT battery connector

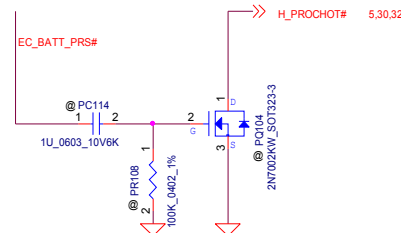
SMART Battery:
 1.GND
 2.GND
 3.BAT_ALERT
 4.SYS_PRES
 5.BATT_PRS
 6.DAT_SMB
 7.CLK_SMB
 8.BATT++
 9.BATT++

Delay adaptor OC H_PROCHOT# 2ms while hybrid power transition



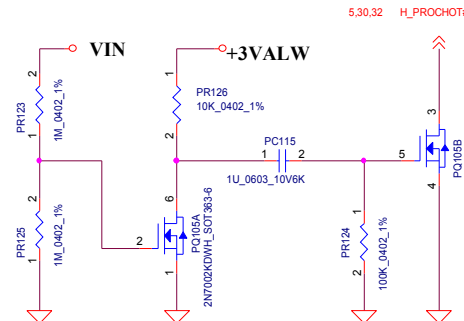
Adaptor protection:

if battery removed, adaptor only, then trigger the H_PROCHOT#, keep DNP in BOM since battery can not be removed by end user



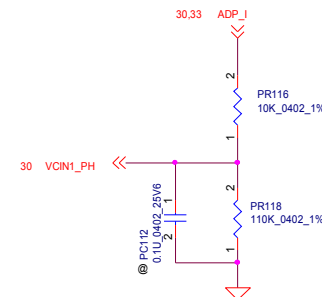
Battery protection:

asserts H_PROCHOT# when adaptor is unplugged, keep low for 10ms till SW_PROCHOT# is issued by EC



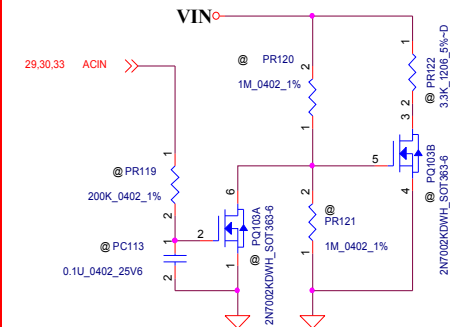
Adaptor protection:

if CP and IPCC failed, adaptor output =rating 100% and over load 20W then trigger the H_PROCHOT# by EC



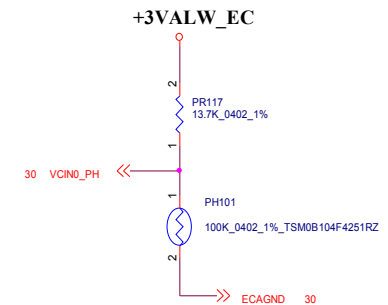
Erp lot6 Circuit

keep DNP in BOM since Dell 45W adaptor has no hiccup mode

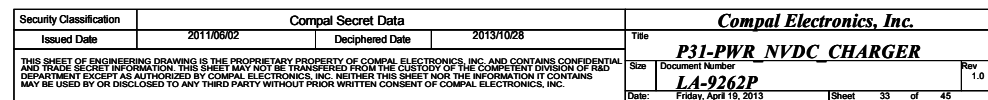


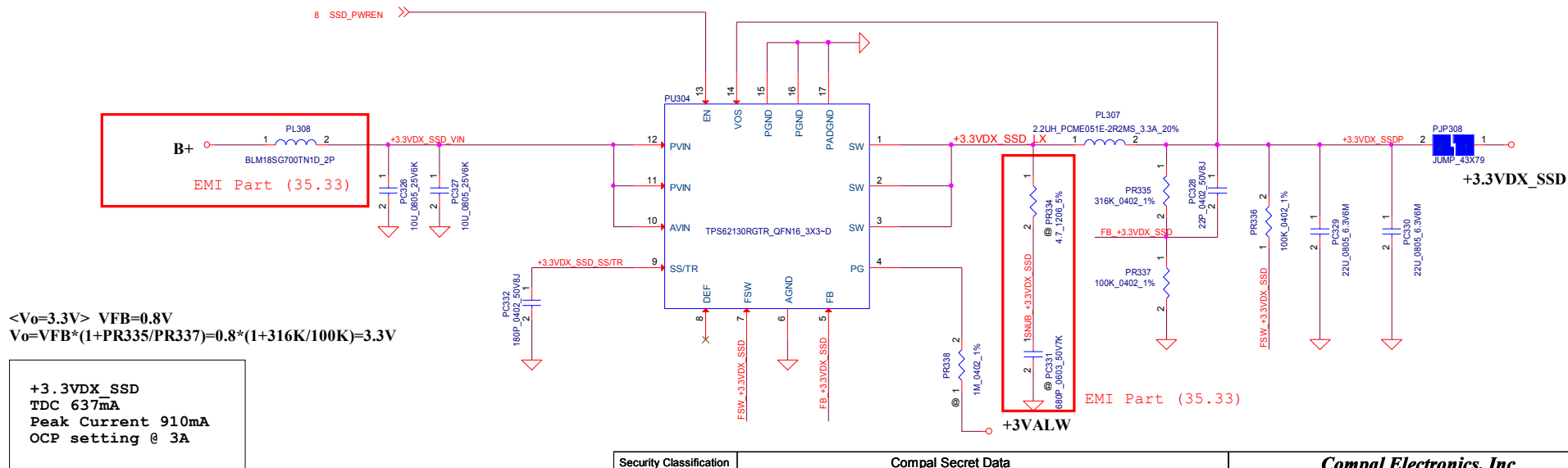
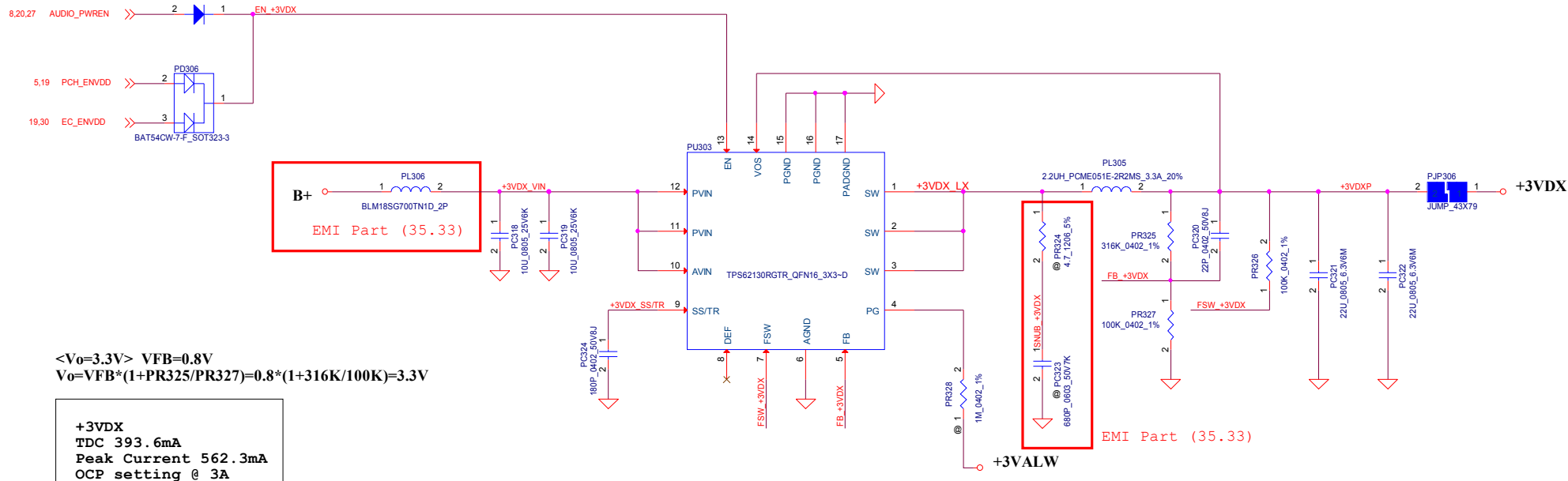
PH101 under CPU bottom side :

CPU thermal protection @88+-3 degree C
 Recovery at 80+-3 degree C

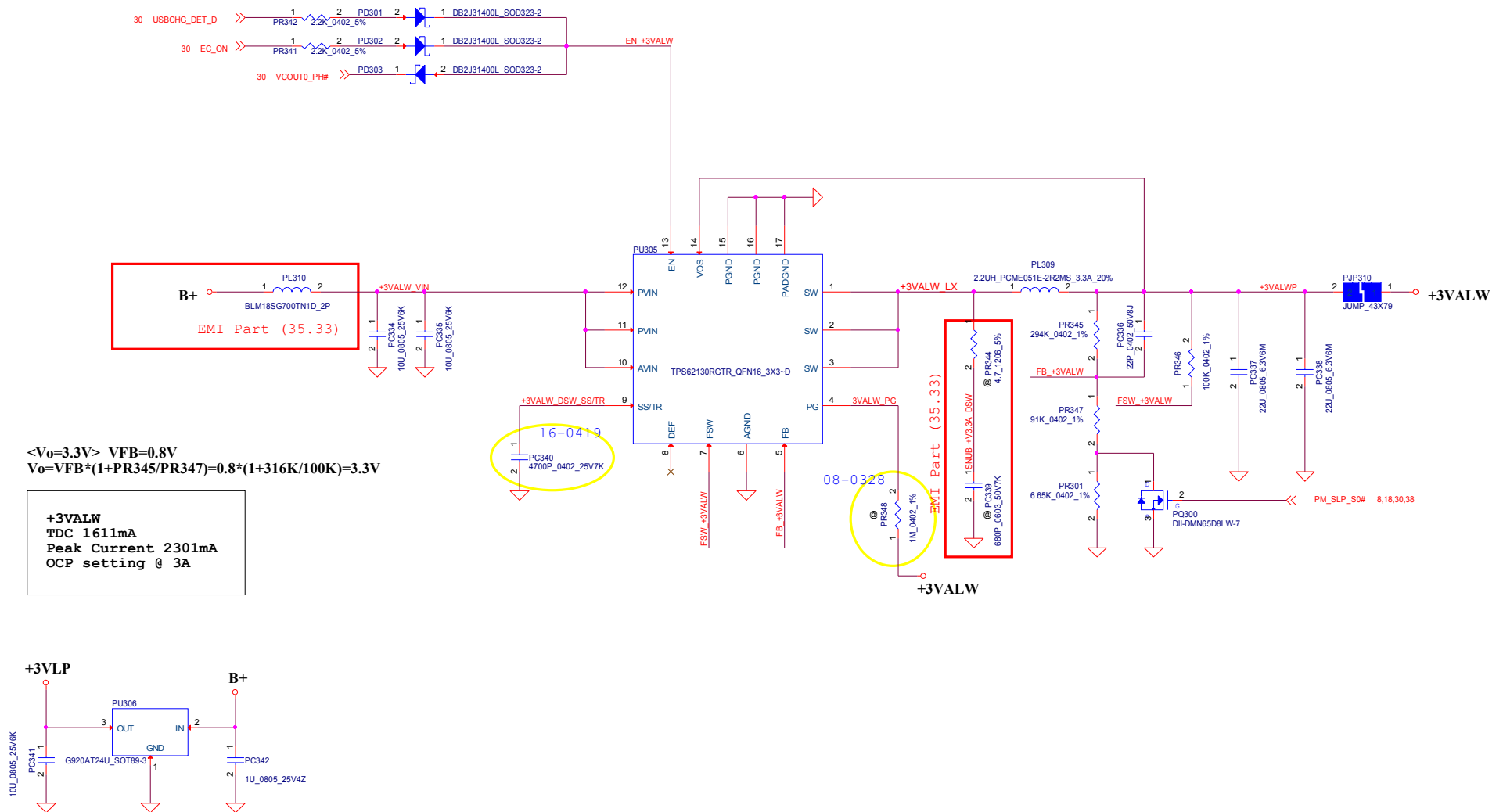


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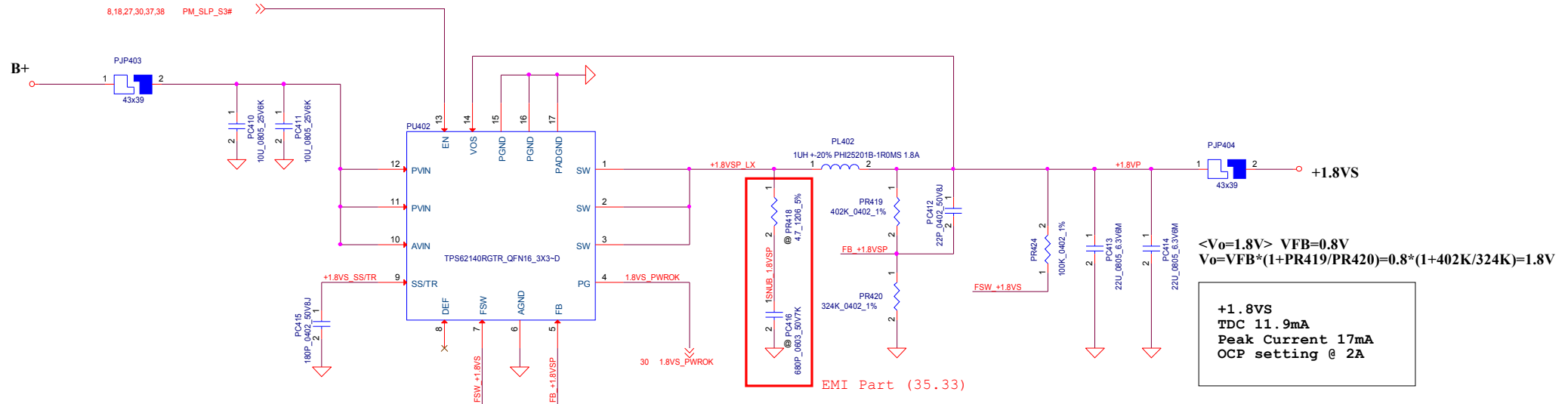
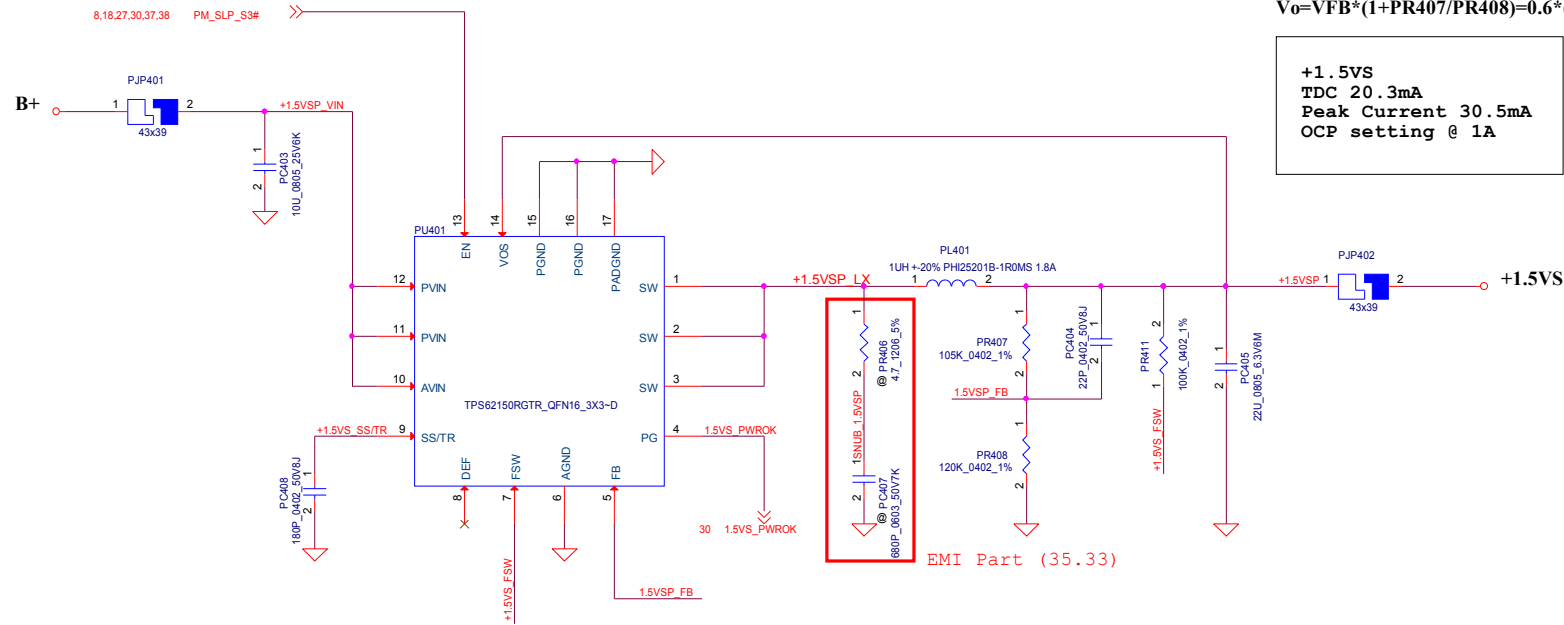




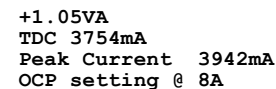
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Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title		
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				Size	Document Number	Rev
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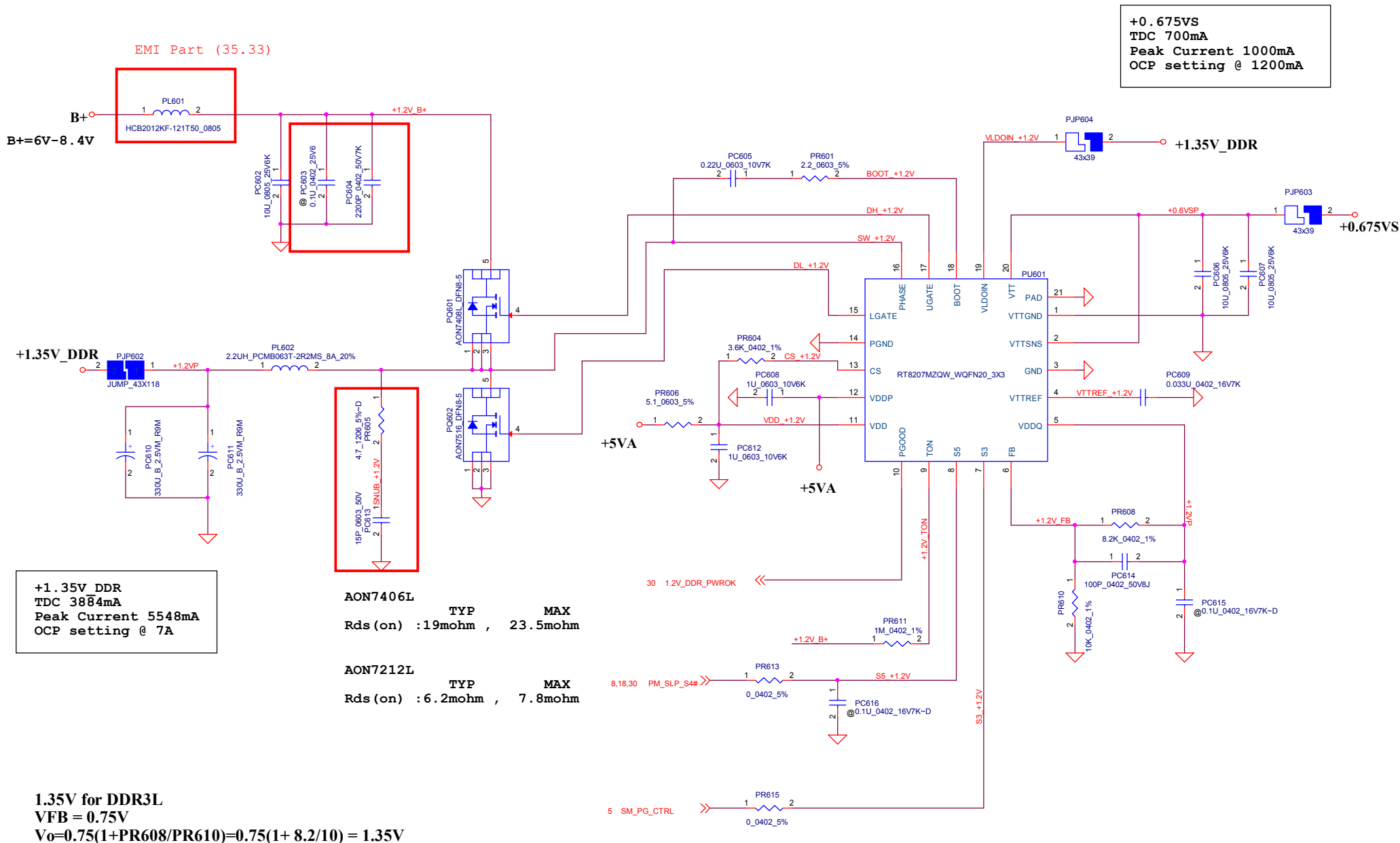
Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title
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				Size Document Number
				LA-9262P
				Rev 1.0
				Date: Friday, April 19, 2013
				Sheet 36 of 45



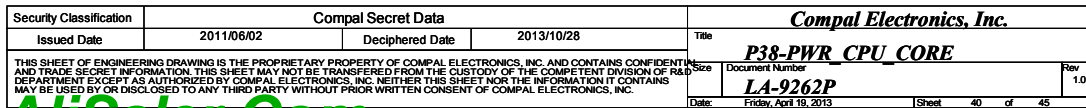
Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/06/02	Deciphered Date	2013/10/28	Title	
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				LA-9262P	
				Date:	Rev
				Friday, April 19, 2013	1.0
				Sheet	37 of 45

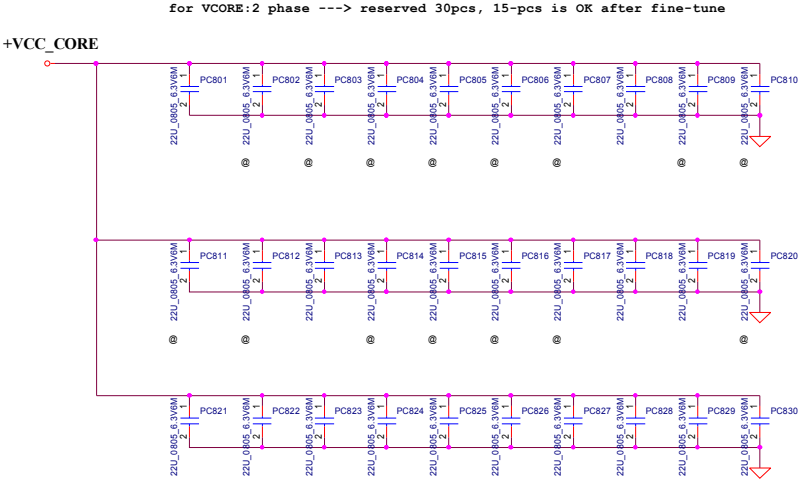


Security Classification		Compal Secret Data		Compal Electronics, Inc. P36-PWR +1.05VS	
Issued Date	2011/06/02	Deciphered Date	2013/10/28		
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				P36-PWR +1.05VS	
				Size	Document Number
				LA-9262P	
				Date:	Friday, April 19, 2013
				Sheet	38 of 45



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Size		Document Number		Rev
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Date:		Friday, April 19, 2013		Sheet 39 of 45





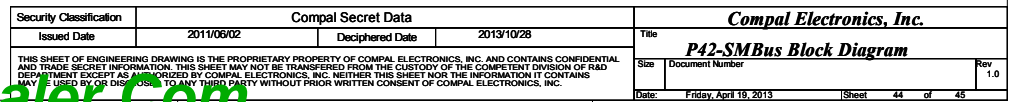
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Issued Date		Deciphered Date		Title		
2011/06/02		2013/10/28		P39-PWR PROCESSOR DECOUPLING		
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Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
X	XX	XXX	XX'XX/XX	Compal_XX	XXXXXX	Change PRXX from Xohm to XXKohm.	
36			20121008	Compal_Power	create one more input cap for TPS51362 Vin	add PC513_10U_0805_16V6K for TPS51362's input	
34			20121012	Compal_HW	create one more resistor for TPS62130 enable pin	add PR342_2.2K_0402_5%	
34			20121018	Compal_Power	design change, delete PU301-PU305, TPS62130 and related components, create PU301, TPS51225 for 3.3V and 5V power rails		
35							
36							
36			20121018	Compal_Power	design change, delete PU401, PU402, TPS62140 and TPS62150 and related components, create PU401and PU402, SY8003D for 1.5V and 1.8V power rails		
34			20121023	dell	reject power design change of 3.3V, 5V, 1.8V and 1.5V		
35							
36							
38			20121203	Compal_EMI	change PL501 for EMI and layout routing	change from SUPPRE_FBMA-L11-453215-800LMA90T_1812 to HCB2012KF-121T50_0805	
39			20121203	Compal_EMI	change PL601 for EMI and layout routing	change from SUPPRE_FBMA-L11-453215-800LMA90T_1812 to HCB2012KF-121T50_0805	
40			20121203	Compal_EMI	add PL703 for EMI	add PL701 HCB2012KF-121T50_0805	
38			20121203	Compal_Power	create PR509 0_0402_5% for debug	add PR509 0_0402_5%	
32			20121205	Compal_HW	create PR5107 10K_0402_1% for test	add PR107 10K_0402_1%	
40			20121213	Compal_Power	fine tune VR transient	de-pop PC714, change PR711 from 150K to be 100K	
40			20130122	Compal_Power	follow Intel's recommendation	change PR737 from 110 OHM to be 130 OHM	
33			20130131	Compal_RF	reserved a MLCC for RF consideration	create PC206 2200P_0402_50V7K	
40			20130221	Compal_RF	for RF noise reducing	pop PC703, PR719 and PC712, PR734 and PC722 for VCORE	
39			20130221	Compal_RF	for RF noise reducing	pop PR605 and PC613 for DDR	

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[Battery only, AC absent]

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